

Main Memory

Review Questions

Section 7.1

- **7.1** What two registers can be used to provide a simple form of memory protection? (
- 7.2 List the three different times at which address binding may occur.
- **7.3** True or False? An address generated by the CPU is also referred to as a physical address.
- 7.4 What is the hardware device that maps virtual to physical addresses?

Section 7.2

- 7.5 What is the backing store?
- **7.6** True or False? Mobile systems typically use swapping.

Section 7.3

- 7.7 What are the three strategies for selecting a free hole from the set of available holes?
- **7.8** What are the two forms of fragmentation?

Section 7.4

7.9 List at least two possible parts of a program that may be assigned separate segments.

Section 7.5

- 7.10 What are the two parts of an address generated by the CPU?
- 7.11 What does each entry in the page table contain?
- **7.12** True or False? Fragmentation can still occur in paging systems.

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7.13 What is the term that describes when a page number is not present in the TLB?

Section 7.6

- **7.14** If a page offset is 13 bits, how large (in bytes) is the page?
- **7.15** How many entries are in a two-level page table with a 20-bit page number?
- **7.16** What is an alternative to hierarchical paging for large (> 32 bits) address sizes?

Section 7.7

- 7.17 True or False? IA-32 address translation involves both paging and segmentation.
- **7.18** True or False? In practice, all 64 bits are used with IA-64 addressing.

Section 7.8

7.19 What are the three components of a 32-bit ARM address?